EE330 Lab 7
Models for MOS Devices

Spring 2024

Contents

Objective

The mathematical relationship between the terminal currents and voltages for a device is termed the device model. Although the basic operation of the MOS transistor is quite straightforward, the task of obtaining a mathematical model for the device that accurately predicts characteristics that can be measured in the laboratory is quite challenging. A large number of models for the MOS transistor have been developed and the research community continues to work on developing even better models.

Although there is considerable ongoing activity on modeling of the MOS transistor, a simple analytical model is widely used for hand calculations and most circuit design activities use the same simple analytical model. This model is often termed the square-law model and for an n-channel transistor is characterized by the equations

$$I_G = I_B = 0$$

$$I_D = \begin{cases} 0 & V_{GS} < V_{THn} \\ \mu_n C_{OX} \dfrac{W}{L}\left(V_{GS} - V_{THn} - \dfrac{V_{DS}}{2}\right)V_{DS} & V_{GS} \geq V_{THn} \text{ and } V_{DS} < V_{GS} - V_{THn} \\ \mu_n C_{OX} \dfrac{W}{2L}\left(V_{GS} - V_{THn}\right)^2 \left(1 + \lambda V_{DS}\right) & V_{GS} \geq V_{THn} \text{ and } V_{DS} \geq V_{GS} - V_{THn} \end{cases} \quad (1)$$

where:

$$V_{THn} = V_{THn0} + \gamma\left(\sqrt{\phi - V_{BS}} - \sqrt{\phi}\right) \quad (2)$$

.

With this model, the device is characterized by the process parameters $\{V_{THn0}, \mu_n C_{OX}, \gamma, \lambda, \varphi\}$ and design parameters {W, L}; the rest are electrical port variables. The parameters μ_n and C_{OX} are actually separate parameters but appear as a product in the model so will be treated as a single model parameter in this experiment. In this experiment assume φ=0.6V.

The functional form of the model for the p-channel transistor is the same but the sign of the drain current is reversed and the mobility and threshold parameters are μ_p and V_{THp}. For the remainder of this experiment, the subscripts n and p will be omitted in the device parameter discussions if from the context it is clear whether reference is with respect to an n-channel or a p-channel transistor.

A more accurate model is the BSIM model used in programs such as SPICE and SPECTRE. The basic BSIM 3 model has 97 parameters but extreme values for the BSIM model parameters (often termed corner models) are often included resulting in a several-fold increase in the total number of parameters. Even this model, however, is often not considered good enough so the concept of

"binning models" is incorporated into existing simulators. A binning BSIM model would be a set of BSIM models that are optimized for a given range of device sizes and operating conditions. The simulator would then select a BSIM model from a model library that has device sizes and operating point close to that of a device in a circuit. The bottom line is that a good BSIM model will typically use several hundred or maybe even a few thousand parameters to characterize a MOS transistor.

The purpose of this laboratory is to develop an understanding of how the square-law model parameters can be extracted. Though this is usually best developed from measured results in this experiment it will be assumed that the transistors can be accurately characterized by the BSIM models. It will take considerably less time to get predicted performance from the BSIM model than it will to take measurements in the laboratory. This approach also makes it practical to investigate models of devices in multiple processes where test devices for in-laboratory measurements are not available. Thus, square-law model parameters will be extracted from the BSIM model and a comparison of the performance of a device with the simpler square-law model and the more complicated BSIM models will be made.

Since the square-law model is less accurate, one would expect that there will be better agreement between the square-law model and the BSIM model when the device is operating close to the point where the model parameters are extracted. Additionally, the deviation between the square-law model and the BSIM model will become significant when the square-law model parameters are used to predict performance of a device with dimensions or operating conditions that differ considerably from the conditions under which the parameters are extracted.

Checkpoints

The checkpoints for this lab are as follows:

1. Completed Pre-Lab
2. Extracted Parameters ($\lambda, \gamma, \mu_n C_{ox}, and\ V_{THn0}$)
3. Square Law Graph
4. Lambda Vs Length Graph
5. [Extra Credit] Early Voltage Plot

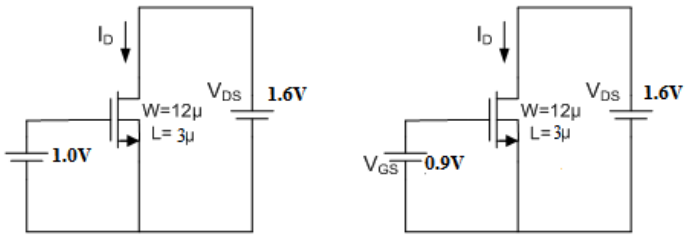
As with all labs, these checkpoints must be shown to a lab TA before the laboratory report is submitted. You should include these checkpoints in your lab report.

Square-Law Parameter Extraction

Extract the process parameters $\{V_{THn0}, \mu_n C_{OX}, \gamma, \lambda\}$ from the BSIM model for an n-channel transistor with dimensions W=12μ and L=3μ near an operating point of V_{GS}=1V, V_{DS}=1.6V, and V_{BS}=0. Note we are only extracting the product $\mu_n C_{OX}$, not the individual parameters μ_n and C_{ox}

To find the operating point current for a circuit, run a DC analysis and only turn on the option of **Save DC operating point.** After successful completion, click on **Results-Print-DC operating points** in the ADE Explorer window. Now click on the transistor in schematic window and you will see the operating point details. The signal called "id" is your drain current.

Hint: One way to extract V_{THn0} would be to simulate the following two circuits (with V_{BS}=0V).



Since both devices are operating in saturation, we obtain the expressions from the two circuits

$$I_{D1} = \mu C_{OX}\left(\frac{W_1}{2L_1}\right)(V_{GS1} - V_{TH})^2(1 + \lambda V_{DS})$$
$$I_{D2} = \mu C_{OX}\left(\frac{W_2}{2L_2}\right)(V_{GS2} - V_{TH})^2(1 + \lambda V_{DS})$$

Since V_{DS} for both circuits are the same, and you can measure I_D and set V_{GS} for each circuit, taking the ratio of these two equations will cancel out the rest of the unknowns, allowing you to find V_{TH}. You can then use Eq. (2) to find V_{TH0}. By using a different V_{BS}, you can use a similar process to find γ.

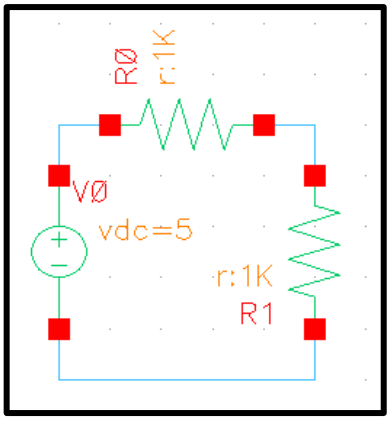
Once you know V_{TH}, you now must find μC_{ox} and λ. You can find one or the other by changing V_{DS} on one of the circuits and then using 2 equations with 2 unknowns where V_{DS} is 1.6V and a V_{DS} of whatever you choose (we recommend 1.8V). Once you find one, then you can plug in and find the other.

Note: In the pre-lab, you were asked to make an Excel sheet to help you calculate process parameters given test data. Use the excel sheet!

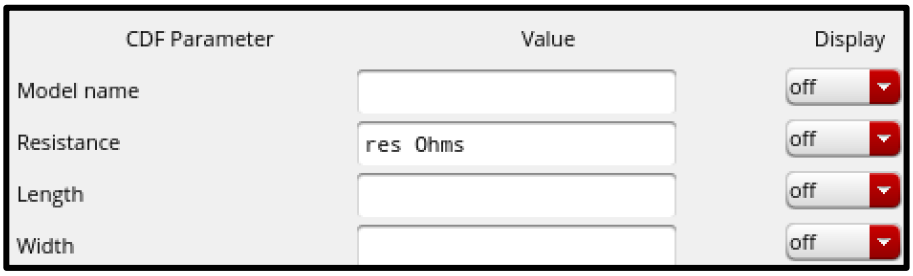
Performing a Parametric Analysis

In the next several sections of the lab, you will need to use the ADE's parametric analysis tool to observe how the current through a MOSFET changes when one of its operating conditions is changed. The content below provides a brief explanation of the ADE's parametric analysis tool and how it can be used. **You do not need to repeat what is done below for your lab; it is simply for illustration purposes.**

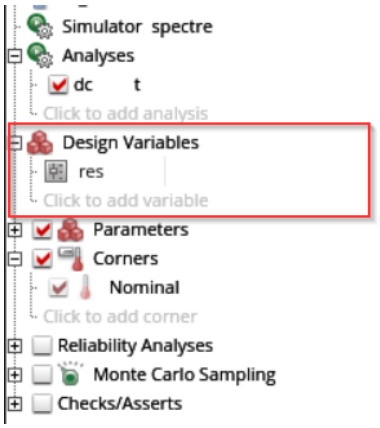
Suppose we have a simple voltage divider circuit, as shown below.



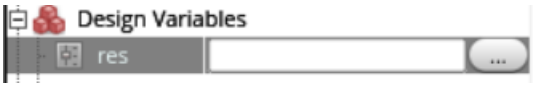
Some time ago, we learned that we could see how the output voltage changes as the input voltage changes using a simple DC analysis which sweeps the DC source's voltage level. But, what if we also want to see how the output changes as R_1 changes? We can achieve this by using the parametric analysis tool to change the schematic properties in our analysis. To do this, we first open the resistor properties and give the parameter we want to change (namely, the resistor's resistance) a variable instead of a value.



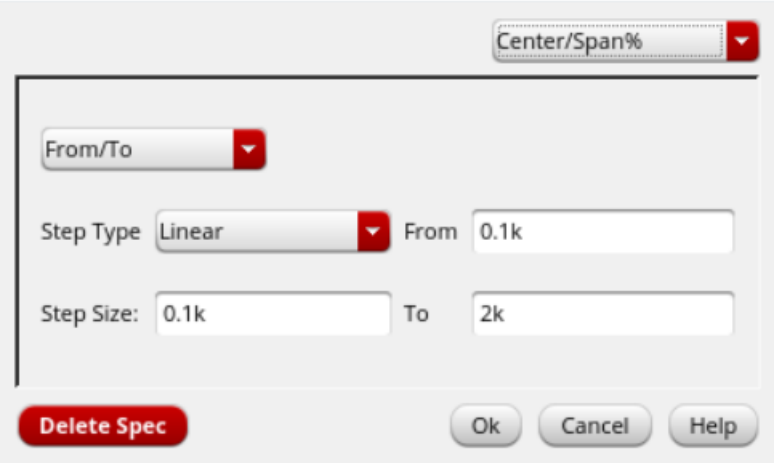
Now, we open our ADE Explorer as usual and add both our input and output voltages to the list of signals to plot, as well as configure out simulation for a DC simulation. On the top bar of the ADE Explorer, there is a section titled "Variables". We can click in this area and click on "Copy from Cellview" to copy all variables in the schematic into our ADE Explorer, resulting in the below setup.



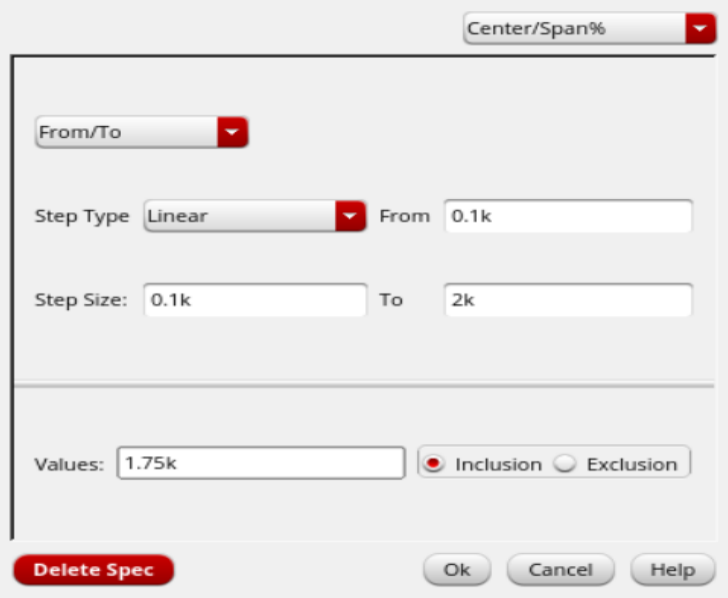
In the cell next to the variable res click to edit and you will see



Click the … to open the variable setup. From the **Add Specification** drop down menu choose **From/To**

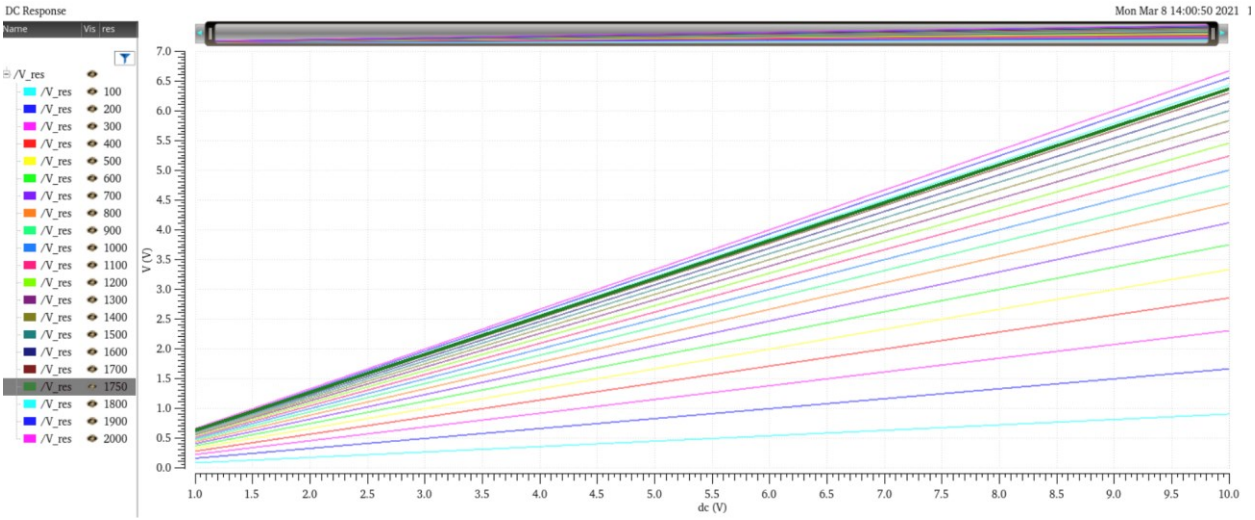


In this example I am sweeping the resistor value form 0.1k to 2k using 0.1k steps. If I want to include a specific value such as 1.75k, I would go back to the drop-down menu and Select **Inclusion List**



After setting up the sweep, click **Ok**

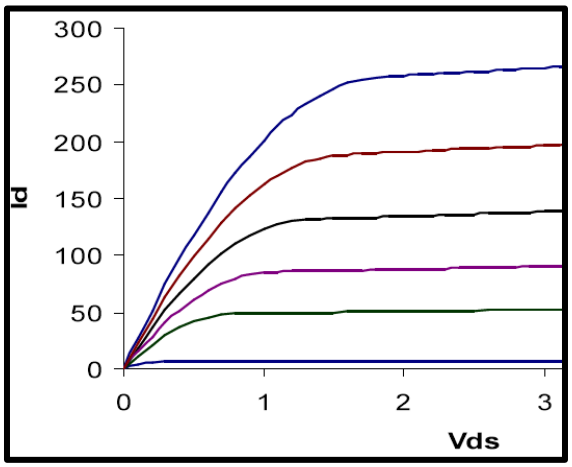
Now, we will just click on the green "run" button. This will take a few seconds to run, but once complete, it'll open a plot with multiple signals in it, as shown below. We can see that we have voltage plots for all resistor values that we wanted to include.



If we wanted, we could add another variable to our schematic and sweep three variables parametrically ($V_{IN}, res1, res2$), but we'll leave that to you to play around with.

MOSFET Output Characteristics

The output characteristics of a MOS transistor are often used to graphically display the transfer characteristics of a device. Typical transfer characteristics of a device are shown below.

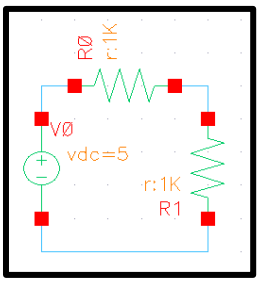


Using the BSIM model and ADE Explorer Design Variable tool, plot the current of a device as a function of drain-source voltage for several (at least 5) gate-source voltages. Do not exceed 2.0V for V_{DS}. Size the device to have dimensions W=12µ and L=3µ. Set V_{BS}=0. You should obtain a family of curves similar to the one shown above.

Choose four points on the plot you have made. Make one point be close to V_{DS}=1.4V and V_{GS}=1V, and the other three points farther away. Now, using the parameters you extracted at the beginning of this lab, calculate the current you expect to flow through the device at each point. Comment on how closely your calculated currents match with the simulated currents. Does your accuracy improve when you're close to your original operating condition (V_{DS}=1.4V, V_{GS}=1V)?

Using the ADE Calculator

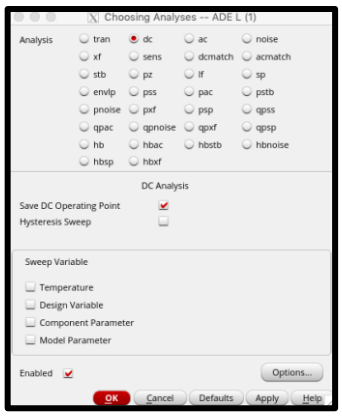
Earlier in this lab, you learned how to perform a parametric analysis in Cadence. In the next section, you will need to use the ADE's calculator function to perform calculations which will then be plotted. The below content provides an overview of how the calculator can be used; **it is not necessary to repeat the example below, although doing so may prove to be good practice.**



Let us return to the voltage divider that we used as an earlier example. In the previous example, we figured out how to plot the output voltage versus input voltage for multiple resistor values. Now, let's say we want to plot the voltage divider ratio of the circuit with multiple resistor values. Recall that the voltage divider ratio is given as follows:

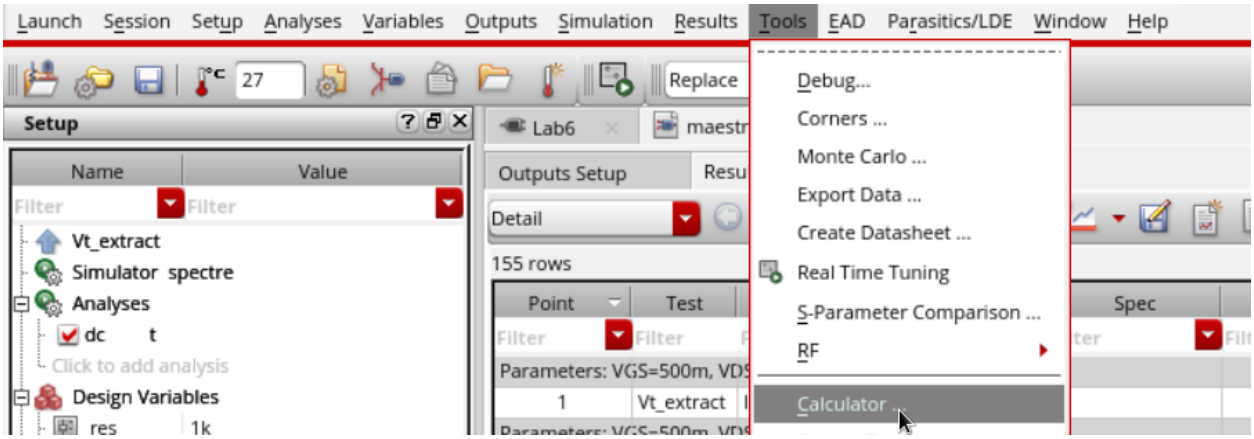
$$n = \frac{R_1}{R_0 + R_1}$$

We can recreate the ADE simulation setup that we did earlier, except without telling the simulation to sweep the voltage; instead, we'll just run a DC analysis and select "Save Operating Point", as shown below. Note that we're also **not** going to plot V_{OUT} and V_{IN}.

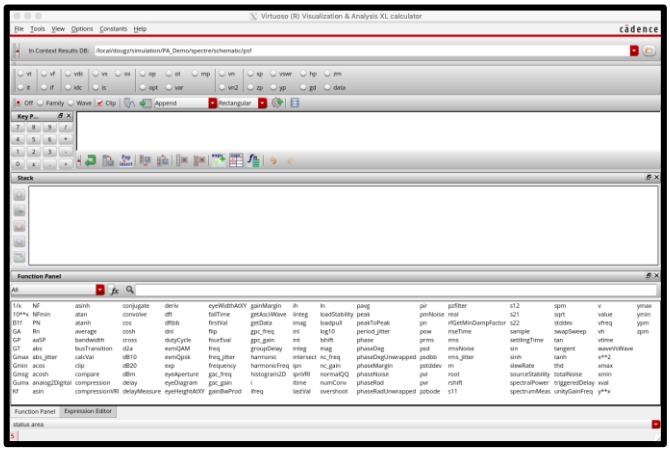


Now, on the left-side of the ADE where our "res" design variable exists, let's give it a value; say, $10k\Omega$. Then, run the simulation. Because we didn't add any signals to plot, nothing will graph. That's OK, because behind the scenes, the ADE just saved a bunch of operating information about the schematic. We need this information to be saved before continuing.

Now that we have saved the operating information, we need to open the ADE Calculator. To do so, in the ADE Explorer window click on **Tools** and then **Calculator.**



This will open a new screen, which is shown below.



The calculator has a lot of features packed into it, so it can be overwhelming at first. Let's start by focusing at the top of the calculator, where a bar of small buttons exists:

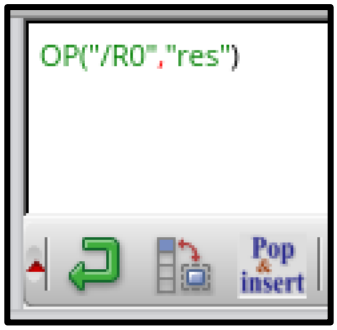
Hovering your mouse over any of these buttons will provide a tooltip explaining what the function will do. Let's go ahead and click on the "op" button. Clicking the button will open the resistor divider schematic as well as a new window:

If you click on the "List" dropdown, nothing will happen. No options will be presented. We need to first click on a component in the schematic, and then click on the "List" dropdown. Doing this will allow us to select an operating point for the component that we clicked. If we click on a resistor, say

R_0, four options will be presented: v, i, res, and pwr. Select the "res" option and then hit "Ok". Notice that the calculator now contains text that says **OP("/R0","res")**.

If no options are presented in the List dropdown after you click on a component, make sure you ran an empty simulation and had the ADE save DC Operating Points.

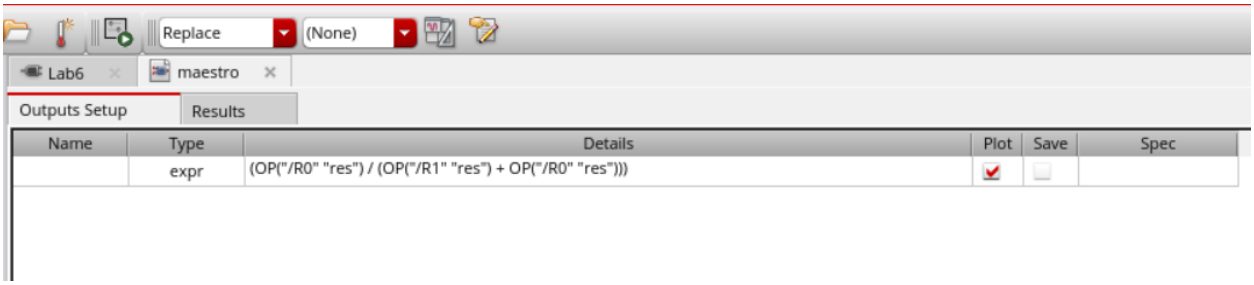
In the ADE Calculator, click on the green "enter" arrow to add the expression to the calculator buffer.



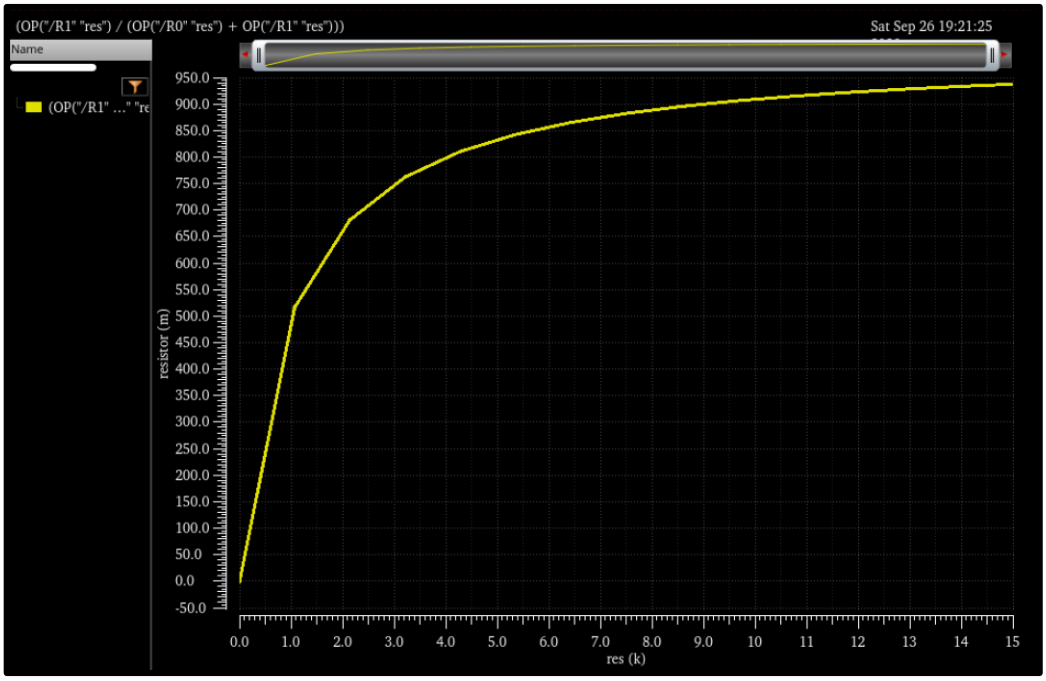
Let's do the same for R_1 so that we have two expressions in the calculator buffer. Once this is done, clear the contents of the expression editor. Drag the OP expression for R_1 into the editor, add a division sign ("/"), an opening parenthesis, and a closing parenthesis. Then, drag the OP expression for R_1 into the parenthesis and add the OP expression for R_2. Your expression should look like this:

Finally, click on the gear and arrow button (highlighted in this image, two from the right) to add the expression to the ADE outputs.

If you close the calculator, your ADE should now look like the image below.



Now, as was done earlier create a parametric analysis which sweeps the “res” variable from one resistance to another. Run the simulation, and you should see a plot of how the resistor divider ratio changes as R_1 changes.



Output Conductance Extraction

As you will soon learn, the small signal output conductance of a MOSFET, as obtained from the square-law model, is given by the following equation:

$$g_0 = \lambda I_{DQ}$$

where g_0 is equivalent to $1/r_{out}$, meaning that λ can be expressed found as follows:

$$\lambda = \frac{1}{r_{out} I_{DQ}}$$

Unfortunately, the parameter λ is quite device size and operating point dependent. Using the ADE Calculator or parametric analysis tools, develop a table of λ values for a wide range of L values and a wide range of operating conditions (small, medium, and large V_{DS} values). Comment on how λ varies with L and with V_{DS}. Support your comments with graphical comparisons. You may find it useful to know that the r_{out} parameter of a NMOS can be found using the “op” option in the calculator.

[Extra Credit] Early Voltage

The parameter λ obtained in Part 1 and used again in Part 3 is related to a parameter called the Early Voltage. In the saturation region, at constant V_{GS} voltages, the drain current I_D varies nearly linearly with V_{DS}. If a line is fit to this drain current, the x-axis intercept of the line is called the Early voltage. Determine the Early Voltage for several I_D-V_{DS} curves. How is the Early Voltage related for the different I_D-V_{DS} curves you obtained? What is the relationship between the Early Voltage and the parameter λ?

Appendix 1

MOSIS WAFER ACCEPTANCE TESTS

RUN: T6AU VENDOR: AMIS
TECHNOLOGY: SCN05 FEATURE SIZE: 0.5 microns
Run type: SKD

INTRODUCTION: This report contains the lot average results obtained by MOSIS from measurements of MOSIS test structures on each wafer of this fabrication lot. SPICE parameters obtained from similar measurements on a selected wafer are also attached.

COMMENTS: American Microsystems, Inc. C5

TRANSISTOR PARAMETERS	W/L	N-CHANNEL	P-CHANNEL	UNITS
MINIMUM	3.0/0.6			
Vth		0.79	-0.92	volts
SHORT	20.0/0.6			
Idss		446	-239	uA/um
Vth		0.68	-0.90	volts
Vpt		10.0	-10.0	volts
WIDE	20.0/0.6			
Ids0		< 2.5	< 2.5	pA/um
LARGE	50/50			
Vth		0.68	-0.95	volts
Vjbkd		10.9	-11.6	volts
Ijlk		<50.0	<50.0	pA
Gamma		0.48	0.58	V^0.5
K' (Uo*Cox/2)		56.4	-18.2	uA/V^2
Low-field Mobility		463.87	149.69	cm^2/V*s

COMMENTS: Poly bias varies with design technology. To account for mask bias use the appropriate value for the parameter XL in your SPICE model card.

Design Technology	XL (um)	XW (um)
SCMOS_SUBM (lambda=0.30)	0.10	0.00
SCMOS (lambda=0.35)	0.00	0.20

FOX TRANSISTORS	GATE	N+ACTIVE	P+ACTIVE	UNITS
Vth	Poly	>15.0	<-15.0	volts

PROCESS PARAMETERS	N+	P+	POLY	PLY2_HR	POLY2	M1	M2	UNITS

Sheet Resistance	83.5	105.3	23.5	999	44.2	0.09	0.10	ohms/sq
Contact Resistance	64.9	149.7	17.3		29.2		0.97	ohms
Gate Oxide Thickness	142							angstrom

PROCESS PARAMETERS	M3	N\PLY	N_W	UNITS
Sheet Resistance	0.05	824	816	ohms/sq
Contact Resistance	0.79			ohms

COMMENTS: N\POLY is N-well under polysilicon.

CAPACITANCE PARAMETERS	N+	P+	POLY	POLY2	M1	M2	M3	N_W	UNITS
Area (substrate)	425	731	84		27	12	7	37	aF/um^2
Area (N+active)			2434		35	16	11		aF/um^2
Area (P+active)			2335						aF/um^2
Area (poly)				938	56	15	9		aF/um^2
Area (poly2)					49				aF/um^2
Area (metal1)						31	13		aF/um^2
Area (metal2)							35		aF/um^2
Fringe (substrate)	344	238			49	33	23		aF/um
Fringe (poly)					59	38	28		aF/um
Fringe (metal1)						51	34		aF/um
Fringe (metal2)							52		aF/um
Overlap (N+active)			232						aF/um
Overlap (P+active)			312						aF/um

CIRCUIT PARAMETERS			UNITS
Inverters	K		
Vinv	1.0	2.02	volts
Vinv	1.5	2.28	volts
Vol (100 uA)	2.0	0.13	volts
Voh (100 uA)	2.0	4.85	volts
Vinv	2.0	2.46	volts
Gain	2.0	-19.72	
Ring Oscillator Freq.			
DIV256 (31-stg,5.0V)		95.31	MHz
D256_WIDE (31-stg,5.0V)		147.94	MHz
Ring Oscillator Power			
DIV256 (31-stg,5.0V)		0.49	uW/MHz/gate
D256_WIDE (31-stg,5.0V)		1.01	uW/MHz/gate

COMMENTS: SUBMICRON

Appendix 2

MOSIS WAFER ACCEPTANCE TESTS

RUN: T4BK (MM_NON-EPI_THK-MTL) VENDOR: TSMC
TECHNOLOGY: SCN018 FEATURE SIZE: 0.18 microns

INTRODUCTION: This report contains the lot average results obtained by MOSIS from measurements of MOSIS test structures on each wafer of this fabrication lot. SPICE parameters obtained from similar measurements on a selected wafer are also attached.

COMMENTS: DSCN6M018_TSMC

TRANSISTOR PARAMETERS	W/L	N-CHANNEL	P-CHANNEL	UNITS
MINIMUM	0.27/0.18			
Vth		0.50	-0.53	volts
SHORT	20.0/0.18			
Idss		571	-266	uA/um
Vth		0.51	-0.53	volts
Vpt		4.7	-5.5	volts
WIDE	20.0/0.18			
Ids0		22.0	-5.6	pA/um
LARGE	50/50			
Vth		0.42	-0.41	volts
Vjbkd		3.1	-4.1	volts
Ijlk		<50.0	<50.0	pA
K' (Uo*Cox/2)		171.8	-36.3	uA/V^2
Low-field Mobility		398.02	84.10	cm^2/V*s

COMMENTS: Poly bias varies with design technology. To account for mask bias use the appropriate value for the parameters XL and XW in your SPICE model card.

Design Technology	XL (um)	XW (um)
SCN6M_DEEP (lambda=0.09)	0.00	-0.01
thick oxide	0.00	-0.01
SCN6M_SUBM (lambda=0.10)	-0.02	0.00
thick oxide	-0.02	0.00

FOX TRANSISTORS	GATE	N+ACTIVE	P+ACTIVE	UNITS
Vth	Poly	>6.6	<-6.6	volts

PROCESS PARAMETERS	N+	P+	POLY	N+BLK	PLY+BLK	M1	M2	UNITS
Sheet Resistance	6.6	7.5	7.7	61.0	317.1	0.08	0.08	ohms/sq
Contact Resistance	10.1	10.6	9.3				4.18	ohms
Gate Oxide Thickness	40							angstrom

PROCESS PARAMETERS	M3	POLY_HRI	M4	M5	M6	N_W	UNITS
Sheet Resistance	0.08	991.5	0.08	0.08	0.01	941	ohms/sq
Contact Resistance	8.97		14.09	18.84	21.44		ohms

COMMENTS: BLK is silicide block.

CAPACITANCE PARAMETERS	N+	P+	POLY	M1	M2	M3	M4	M5	M6	R_W	D_N_W	M5P	N_W	UNITS
Area (substrate)	998	1152	103	39	19	13	9	8	3		129		127	aF/um^2
Area (N+active)			8566	54	21	14	11	10	9					aF/um^2
Area (P+active)			8324											aF/um^2
Area (poly)				64	18	10	7	6	5					aF/um^2
Area (metal1)					44	16	10	7	5					aF/um^2
Area (metal2)						38	15	9	7					aF/um^2
Area (metal3)							40	15	9					aF/um^2
Area (metal4)								37	14					aF/um^2
Area (metal5)									36			1003		aF/um^2
Area (r well)	987													aF/um^2
Area (d well)										574				aF/um^2
Area (no well)	139													aF/um^2
Fringe (substrate)	244	201		18	61	55	43	25						aF/um
Fringe (poly)				69	39	29	24	21	19					aF/um
Fringe (metal1)					61	35		23	21					aF/um
Fringe (metal2)						54	37	27	24					aF/um
Fringe (metal3)							56	34	31					aF/um
Fringe (metal4)								58	40					aF/um
Fringe (metal5)									61					aF/um
Overlap (P+active)			652											aF/um

CIRCUIT PARAMETERS			UNITS
Inverters	K		
Vinv	1.0	0.74	volts
Vinv	1.5	0.78	volts
Vol (100 uA)	2.0	0.08	volts
Voh (100 uA)	2.0	1.63	volts
Vinv	2.0	0.82	volts
Gain	2.0	-23.33	
Ring Oscillator Freq.			
D1024_THK (31-stg,3.3V)		338.22	MHz
DIV1024 (31-stg,1.8V)		402.84	MHz
Ring Oscillator Power			
D1024_THK (31-stg,3.3V)		0.07	uW/MHz/gate
DIV1024 (31-stg,1.8V)		0.02	uW/MHz/gate

COMMENTS: DEEP_SUBMICRON